End Sem (I) – MCA (I)

2017

Time: 3 hours

Full Marks: 70

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Answer from **all** the Groups are directed.

Group – A

(**Compulsory**)

1. [A] Correct the statements as **True** or **False**:   1x15=15
    a) AND gate has only one output.
    b) Registers consist of Latches.
    c) Digital Counters consist of number of flip-flop.
    d) Boolean algebra is an algebra of logic.
    e) Direct addressing is the address of data specified within the instruction itself.

    [B] Convert the following:
    a) $(11110110111)_2 = (?)_{10}$
    b) $(46.57)_8 = (?)_{16}$
    c) $(376)_8 = (?)_2$
    d) $(3DE)_{16} = (?)_2$
    e) $(1101.1010)_2 = (?)_{10}$

[C] Change the following conversions into:

a) 1^s complement:
   a. 101100
   b. 11001
b) 2^s complement: 0000
c) 9^s complement: 75
d) 10^s complement: 183

Group – B

Answer any **five** questions of the following: 4x5=20

2. What is Flip-Flop? Explain JK flip-flop with diagram.
3. What is MUX and DMUX? Explain.
4. Differentiate between Magnetic disk and Hard disk?
5. Evaluate $\overline{XY} + \bar{X}Z + YZ + \bar{Y}Z\bar{W}$.
6. Explain NAND is Universal Gate.
7. Explain the structure of Von-Neumann architecture.
8. What is addressing mode? Explain its types.

Group – C

Answer any **five** questions of the following: 7x5=35

9. Describe the structure of Microprocessor (8085) with neat and clean diagram.
10. What is Pipelining? Describe its features. What are the main differences between CISC and RISC?
11. Describe Sequential Circuit. How it is differ from Combinational Circuit.

12. Write short notes on the following:
    a) ROM and its types
    b) Micro-programmed control
    c) K-map
13. What is the function of a Cache Memory? Explain the term cache hit and cache miss.
14. Describe DMA Controller with neat and clean diagram. Explain its features.
15. What is Logic Gates? Describe its various types.

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